SPECIFICATION

At page 4, line 23, replace the existing paragraph with the following.

—Unlike the system 500, however, the system 700 includes a memory module 716. The memory module 716 might include an edge connector 714 comprising a plurality of contact pads (not shown), a plurality of memory devices (708), a module board (706), and a C/A buffer (710). The contact pads are typically present at both sides of the board 706. A plurality of receptacles, e.g., sockets 712, is mounted on the motherboard 502. The sockets 712 receive the edge connectors 714 to thereby electrically couple the motherboard 502 to the memory module 716. More particularly, the sockets 712 electrically couple traces routed on the motherboard 502 to traces routed on the module board 706 such that the memory module 716 is coupled to the motherboard 502 and the controller ~~704~~ 504.—

At page 4, line 32, replace the existing paragraph with the following.

—The memory module 716 includes a plurality of memory devices 708. These memory devices 708 are, for example, DRAM and SDRAM. A buffer 710 controls and buffers commands and addresses it receives from the memory controller ~~704~~ 504. The plurality of memory devices 708 and the buffer 710 are mounted on the module board 706. —

At page 5, line 3, replace the existing paragraph with the following.

— In one embodiment, the memory module 716 is positioned farthest from the controller ~~704~~ 504. Doing so, eliminates signal reflection because there exists no branch point from signal traces on the motherboard 702. That is, the branch point causes a signal to be transferred in as many directions as points emanating from the branch point, e.g., two or more directions. Undesired signal reflection might occur because of mismatching of a characteristic impedance (Z0) at the branch point.—

At page 5, line 9, replace the existing paragraph with the following.

—The signal path between the controller ~~704~~ 504 and the memory module 716 extends from the controller ~~704~~ 504 to the memory 708 to the memory module 716. Since the memory 708 is soldered directly to the board 706, no signal branch exists at that point and, therefore, no signal reflection. On the other hand, if the memory module 716 is positioned between the

controller ~~704~~ 504 and memory 708, the connector socket must be located between the signal trace creating a stub or branch from the module trace. This branch will create a signal reflection.—

At page 6, line 1, replace the existing paragraph with the following.

—Figure 10 is a top view of an embodiment of a memory system 1000 according to the present invention. The system 1000 is substantially similar to the system 900 with the addition of a memory module ~~706~~ 716. The memory module 716 operates substantially as described earlier with reference to Figure 7. The memory module 716 includes a PLL 720 that is capable of generating a first clock 1stCLK responsive to the system clock CLK and a module board 706. The PLL 720 provides the 1stCLK signal to its corresponding memory devices 708 on the memory module 716. By adding the PLL 720, the system 1000 avoids having to route the system clock separately to each memory device 508, 708 from the memory controller 504. In another embodiment, the PLL 520, 720 might likewise be replaced with a delay locked loop (DLL) that operates similarly to the PLL 520, 720. That is, the DLL is capable of generating the 1stCLK responsive the system clock CLK and to provide the 1stCLK to its corresponding memory devices 508, 708.—